

AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Currently Amended) A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period which stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen; and

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal,

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits.

2. (Original) The display device as set forth in claim 1, further comprising:

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and the driving control circuit stops driving of the output timing clock generation circuit in the inaction period.

3. (Currently Amended) The display device as set forth in claim 2, further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the output timing clock generation circuit generates the output timing clock based on the start timing clock generated in the start timing clock generation circuit, and the driving control circuit stops driving of the start

timing clock generation circuit in the inaction period, based on the control clock signal.

4. (Original) The display device as set forth in claim 1, wherein:
the clock signal generation circuit is a clock signal oscillation circuit for
oscillating a clock signal.

5. (Original) The display device as set forth in claim 1, wherein:
liquid crystal display elements are used as the pixels.

6. (Currently Amended) A driving method for a display device which
selects each line of a screen having pixels aligned in a matrix manner by
applying a scanning signal to a scanning signal line of a pixel of each line so as
to scan the screen, and supplies a data signal from a data signal line to a pixel
of a selected line so as to carry out display, the driving method comprising:
generating, as a driving control signal, a control clock signal that
defines an inaction period where all scanning signal lines become non-
scanning state, the inaction period being provided between scanning periods
for scanning the screen; and
stopping driving of a clock signal generation circuit in the inaction
period, the clock signal generation circuit being for generating a clock signal
which is used for taking the data signal into the data signal line, the clock
signal being faster than the control clock signal.

wherein:

~~an inaction period is provided between the scanning periods for scanning the screen, and driving of a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line is stopped in the inaction period.~~

7. (New) The display device as set forth in claim 1, further comprising:

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit.

8. (New) The display device as set forth in claim 7, further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the start timing clock generation circuit generates the start timing clock based on the output timing clock generated in the output timing clock generation circuit.

9. (New) The display device as set forth in claim 8, wherein:
the driving control circuit generates the control clock signal based on the
start timing clock generated by the start timing clock generation circuit.
10. (New) The display device as set forth in claim 2, further comprising:
a start timing clock generation circuit for generating a start timing clock
which is used as a scanning start timing signal of the driving circuits,
wherein:
the output timing clock generation circuit generates the output timing
clock based on the start timing clock generated in the start timing clock
generation circuit.
11. (New) The display device as set forth in claim 10, wherein:
the driving control circuit generates the control clock signal based on the
start timing clock generated by the start timing clock generation circuit.
12. (New) The display device as set forth in claim 1, wherein:
the clock signal generation circuit generates the clock signal based on
the control clock signal generated by the driving control circuit.
13. (New) The display device as set forth in claim 12, further
comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the output timing clock generation circuit generates the output timing clock from the control clock signal generated by the driving control circuit.

14. (New) The display device as set forth in claim 13, further comprising:

an output timing clock generation circuit for generating an output timing clock which is sued as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal from the output timing clock generated by the output timing clock generation circuit.

15. (New) The display device as set forth in claim 14, further comprising:

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits; and

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the start timing clock generation circuit generates the start timing clock from the output timing clock generated in the output timing clock generation circuit.

16. (New) The display device as set forth in claim 15, wherein:
the driving control circuit generates the control clock signal based on the start timing clock generated by the start timing clock generation circuit.